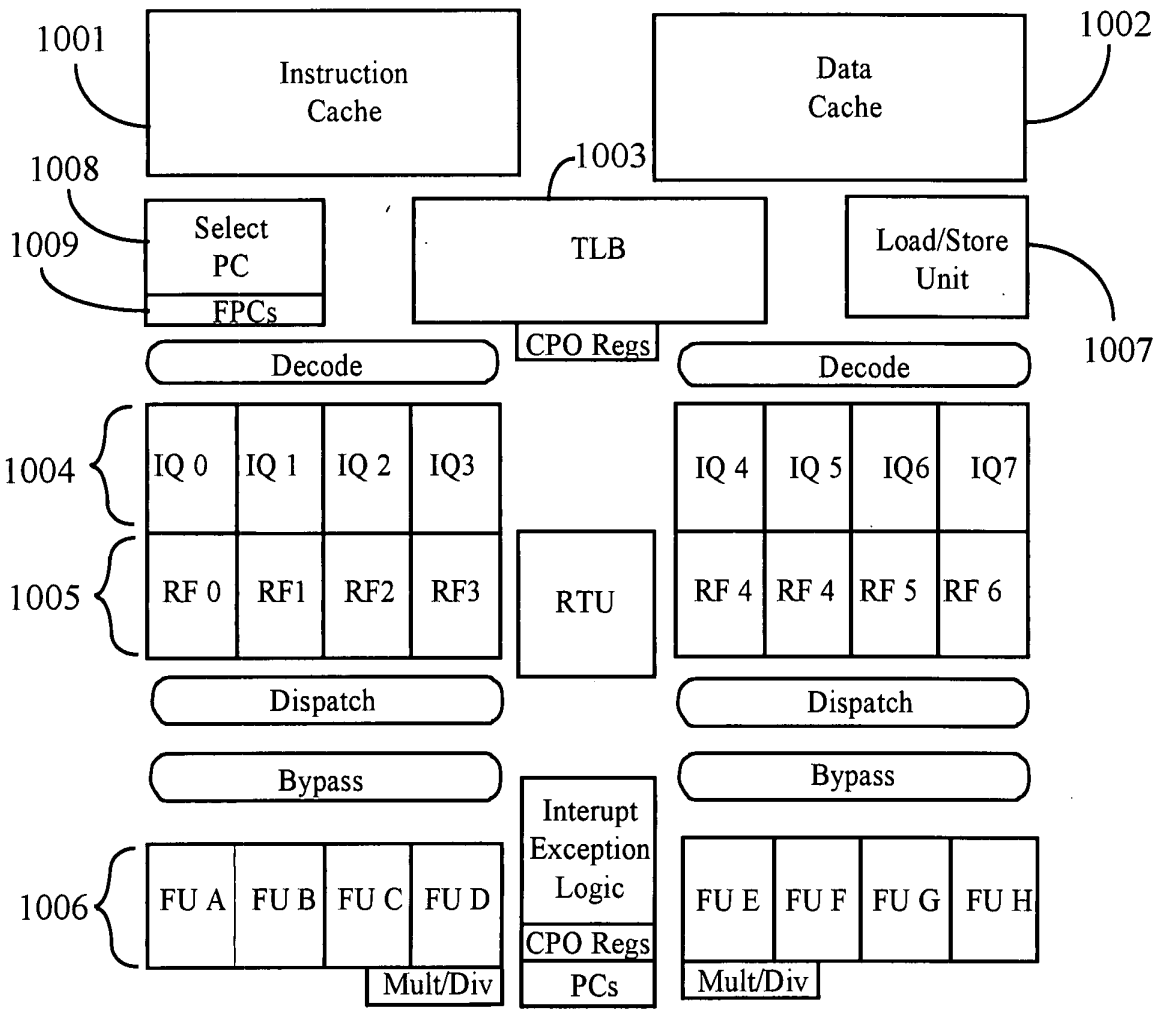
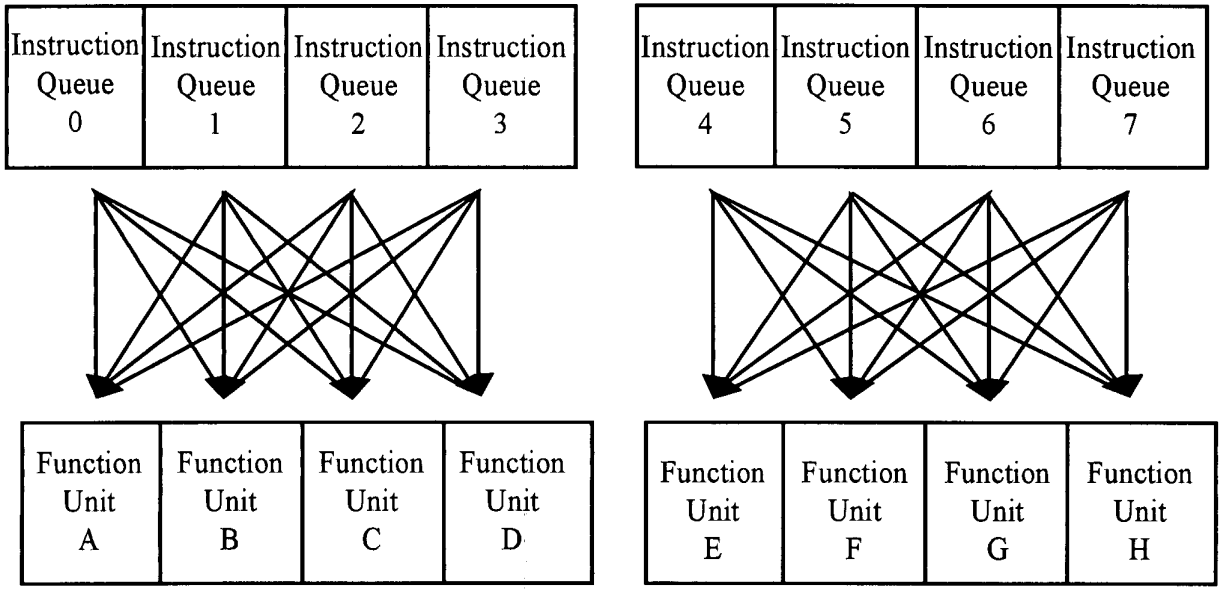


SPU Block Diagram

Fig. 1

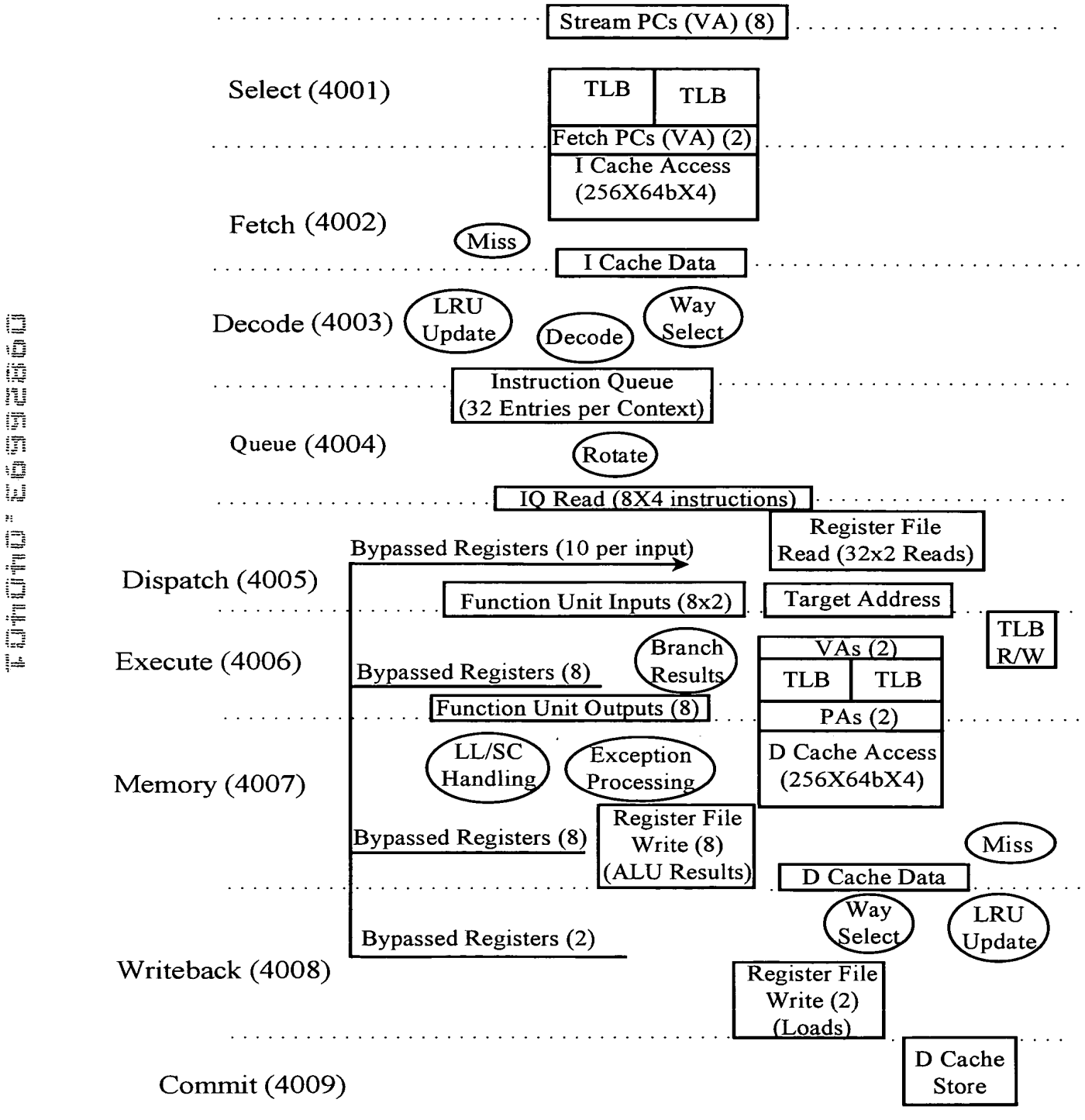
	New LRU bits					
Way Accessed	0-MRU-1	0-MRU-2	0-MRU-3	1-MRU-2	1-MRU-3	2-MRU-3
0	1	1	1	N/C	N/C	N/C
1	0	N/C	N/C	1	1	N/C
2	N/C	0	N/C	0	N/C	1
3	N/C	N/C	0	N/C	0	0
0,1	X	1	1	1	1	N/C
0,2	1	X	1	0	N/C	1
0,3	1	1	X	N/C	0	0
1,2	0	0	N/C	X	1	1
1,3	0	N/C	0	1	X	0
2,3	N/C	0	0	0	0	X

Fig. 2



Function Unit Dispatch Pattern

Fig. 3



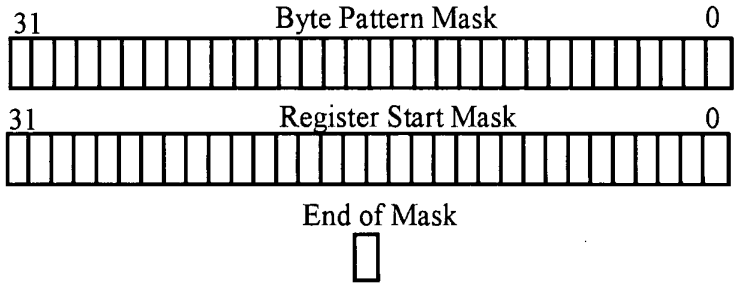
Pipeline Timing Diagram

Fig. 4

31 26	25 21	20 16	15 11	10 6	5 0
Special 0000000	RS	RT	MASK	LDX 00000	XSTREAM 110111
Special 0000000	RS	RT	MASK	STX 00001	XSTREAM 110111

Masked Load/Store Instructions

Fig. 5



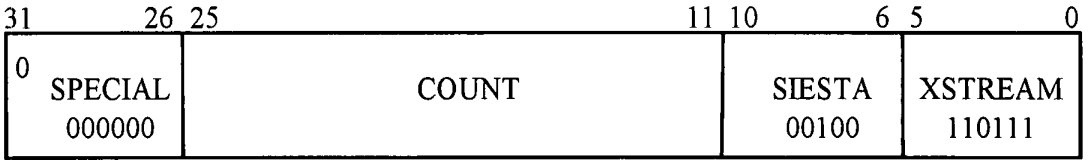
LDX/STX Mask Registers

Fig. 6

31 26	25 21	20 16	15 11	10 6	5 0
Special 0000000	RS	RT	RD	ADDX 00010	XSTREAM 110111
Special 0000000	RS	RT	RD	SUBX 00011	XSTREAM 110111

Special Arithmetic Instructions

Fig. 7



Siesta Instruction

Fig. 8

31 26	25 21	20 16	15 11	10 6	5 0
Special 0000000	RS	00000	RD	GETSPC 10000	XSTREAM 110111
Special 0000000	RS	00000	00000	FREESPC 10001	XSTREAM 110111

PMU - Packet Memory Instructions

Fig. 9

31 26	25 21	20 16	15 11	10 6	5 0
Special 0000000	RS	00000	00000	PKTEXT 10010	XSTREAM 110111
Special 0000000	RS	RT	RD	PKTINS 10011	XSTREAM 110111
Special 0000000	RS	RT	00000	PKTDONE 10100	XSTREAM 110111
Special 0000000	RS	RT	00000	PKTMOVE 10101	XSTREAM 110111
Special 0000000	RS	RT	00000	PKTUPD 10110	XSTREAM 110111
Special 0000000	RS	RT	ITEM	PKTPR 10111	XSTREAM 110111
Special 0000000	RS	RT	00000	PKTMAR 11010	XSTREAM 110111
Special 0000000	RS	000000	RD	PKTACT 11011	XSTREAM 110111

PMU - Queuing System Instructions

Fig. 10

31 26	25 21	20 16	15 11	10 6	5 0
Special 0000000	00000	00000	00000	RELEASE 11000	XSTREAM 110111
Special 0000000	RS	00000	RD	GETCTX 11001	XSTREAM 110111

PMU - RTU Instructions

Fig. 11

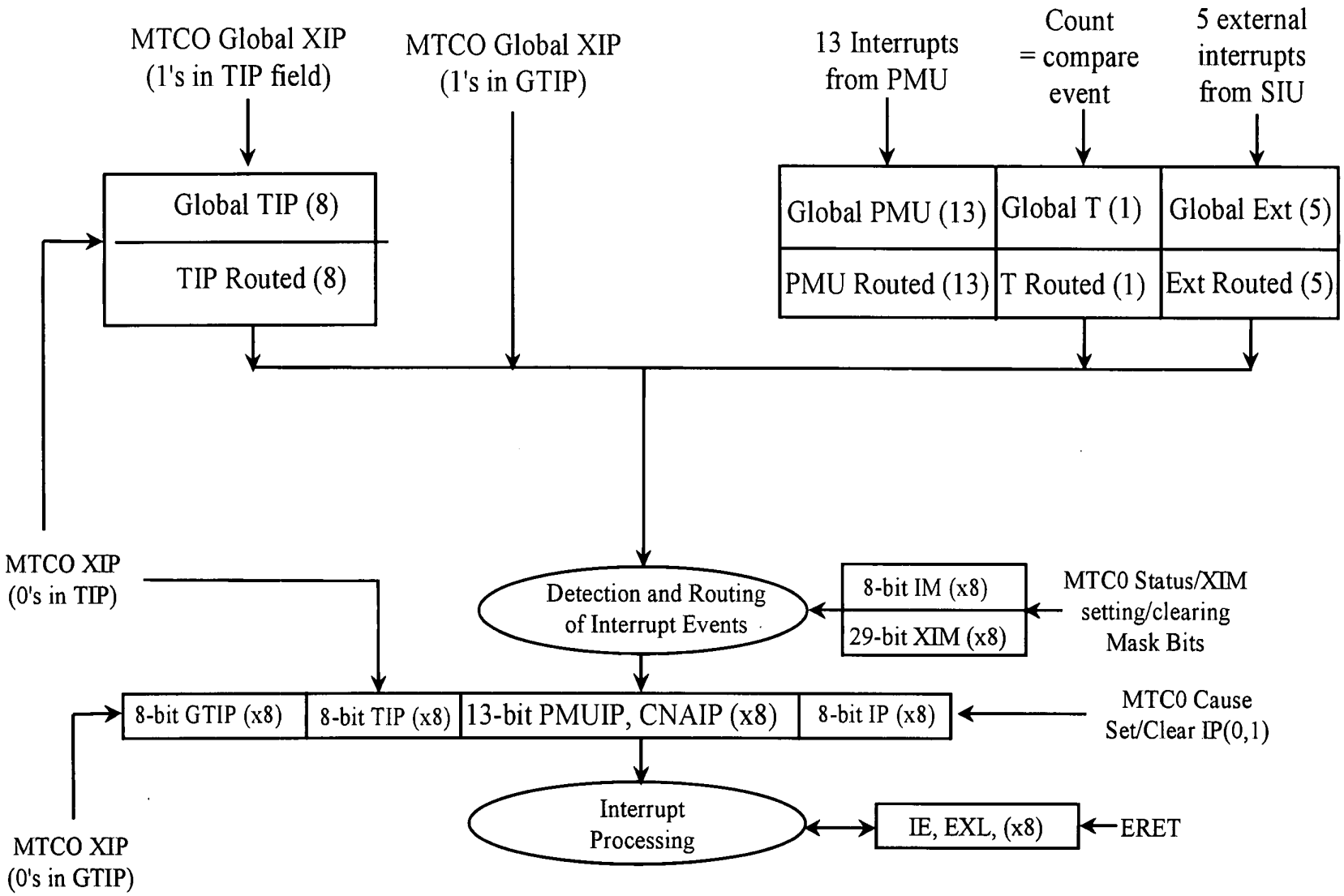
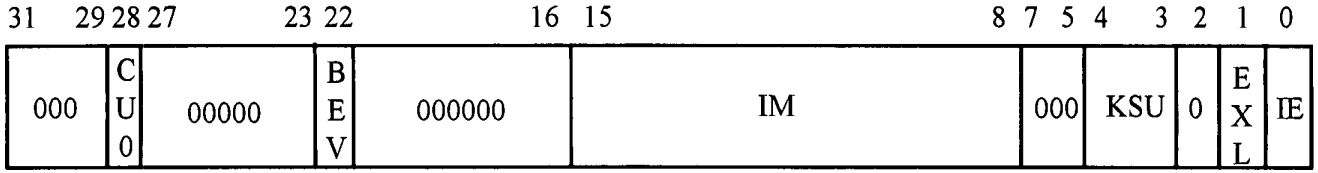
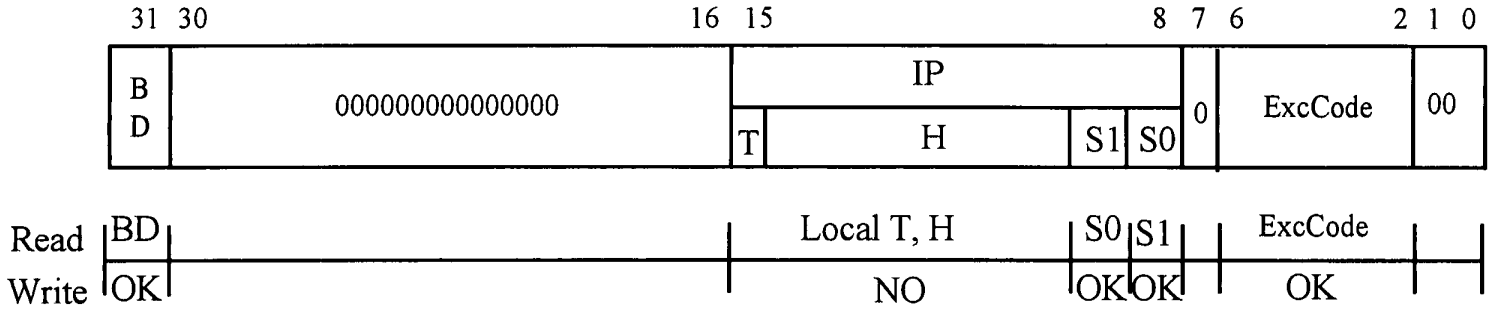

MTCO Global XIP
(1's in TIP field)
MTCO Global XIP
(1's in GTIP)
13 Interrupts
from PMU
Count
= compare
event
5 external
interrupts
from SIU
Global TIP (8)
TIP Routed (8)
Global PMU (13)
PMU Routed (13)
Global T (1)
T Routed (1)
Global Ext (5)
Ext Routed (5)
MTCO XIP
(0's in TIP)
Detection and Routing
of Interrupt Events
8-bit IM (x8)
29-bit XIM (x8)
MTC0 Status/XIM
setting/clearing
Mask Bits
8-bit GTIP (x8)
8-bit TIP (x8)
13-bit PMUIP, CNAIP (x8)
8-bit IP (x8)
MTC0 Cause
Set/Clear IP(0,1)
Interrupt
Processing
IE, EXL, (x8)
ERET
MTCO XIP
(0's in GTIP)

Fig. 12



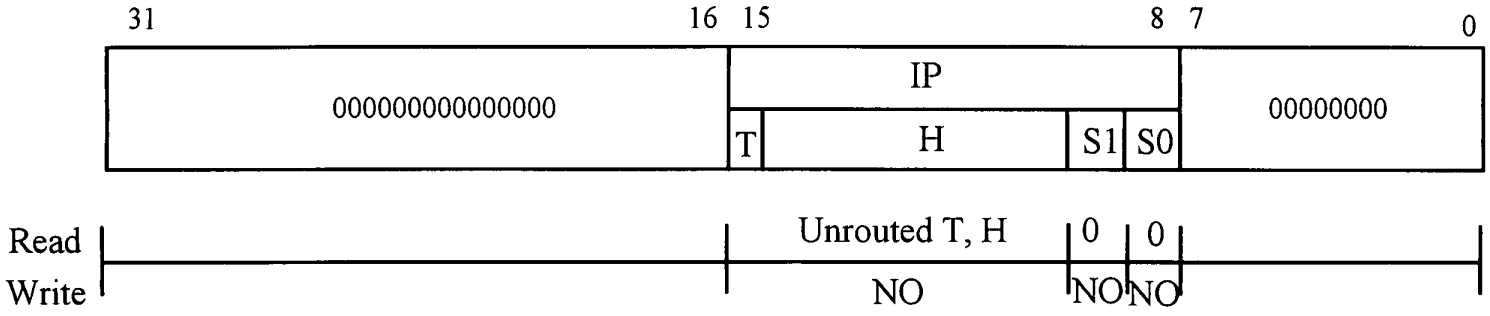
Status Register

Fig. 13



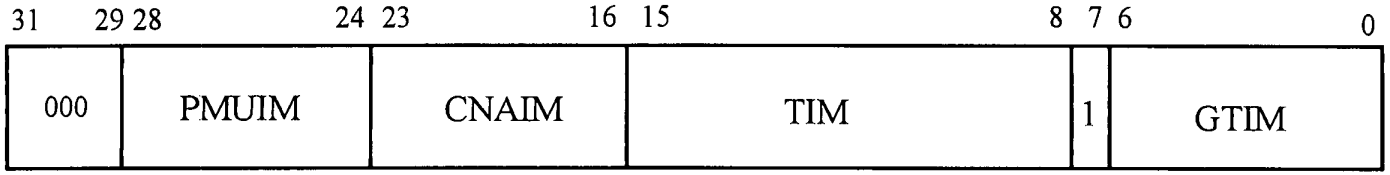
Cause Register

Fig. 14



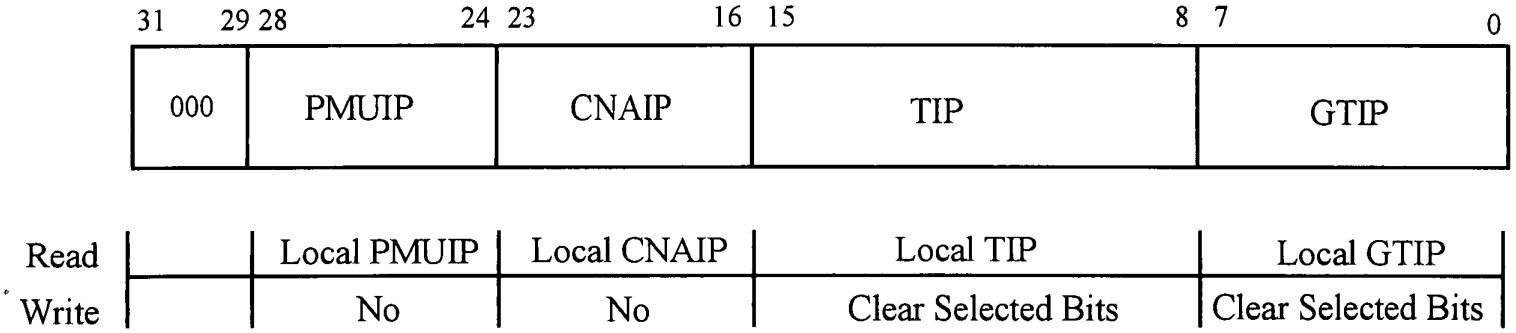
Global Cause Register

Fig. 15



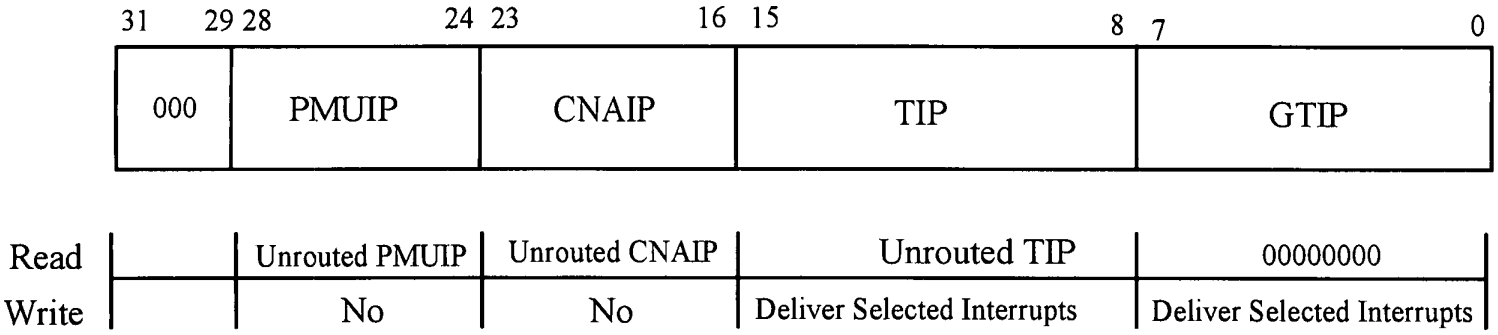
Extended Interrupt Mask Register

Fig. 16



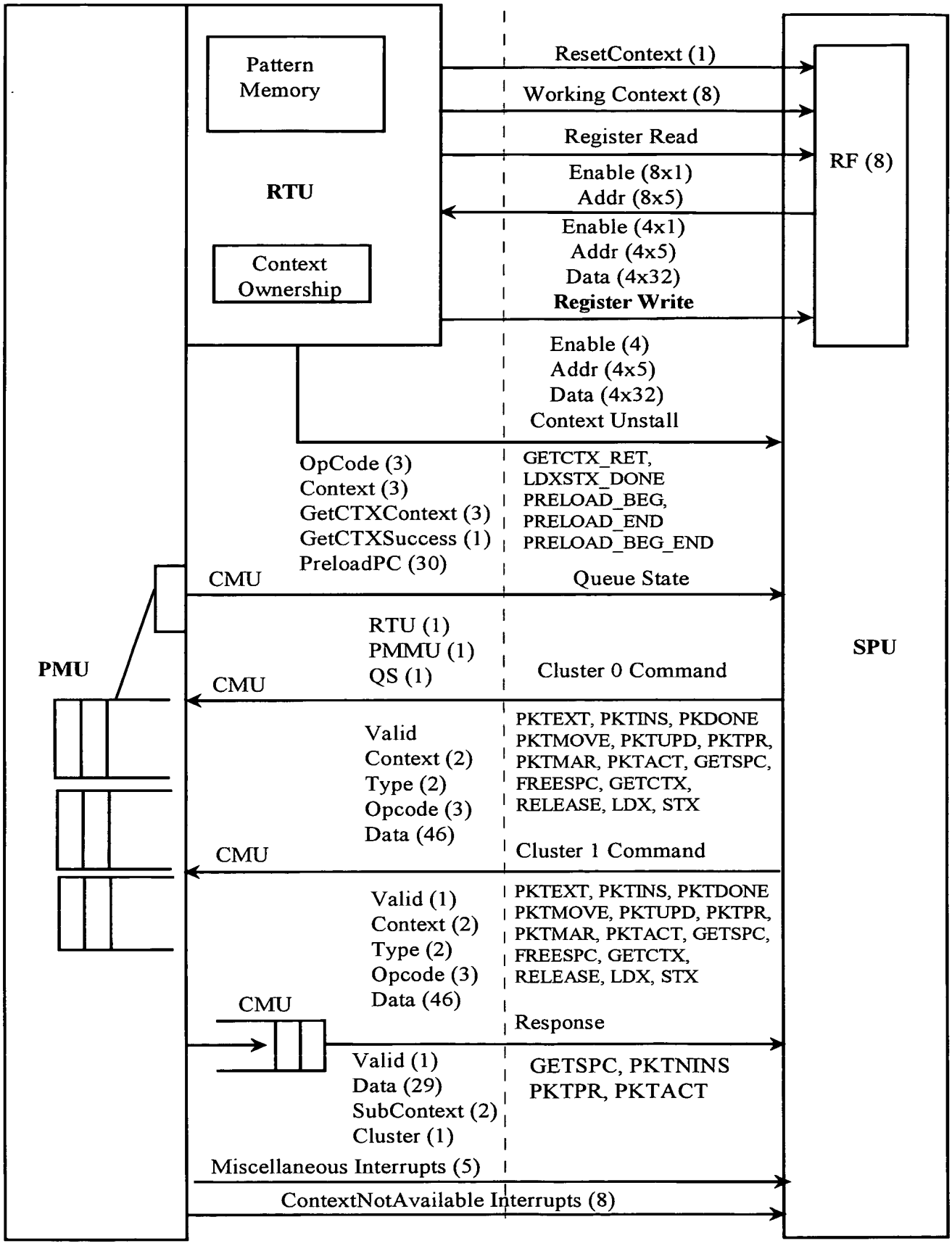
Extended Interrupt Pending Register

Fig. 17



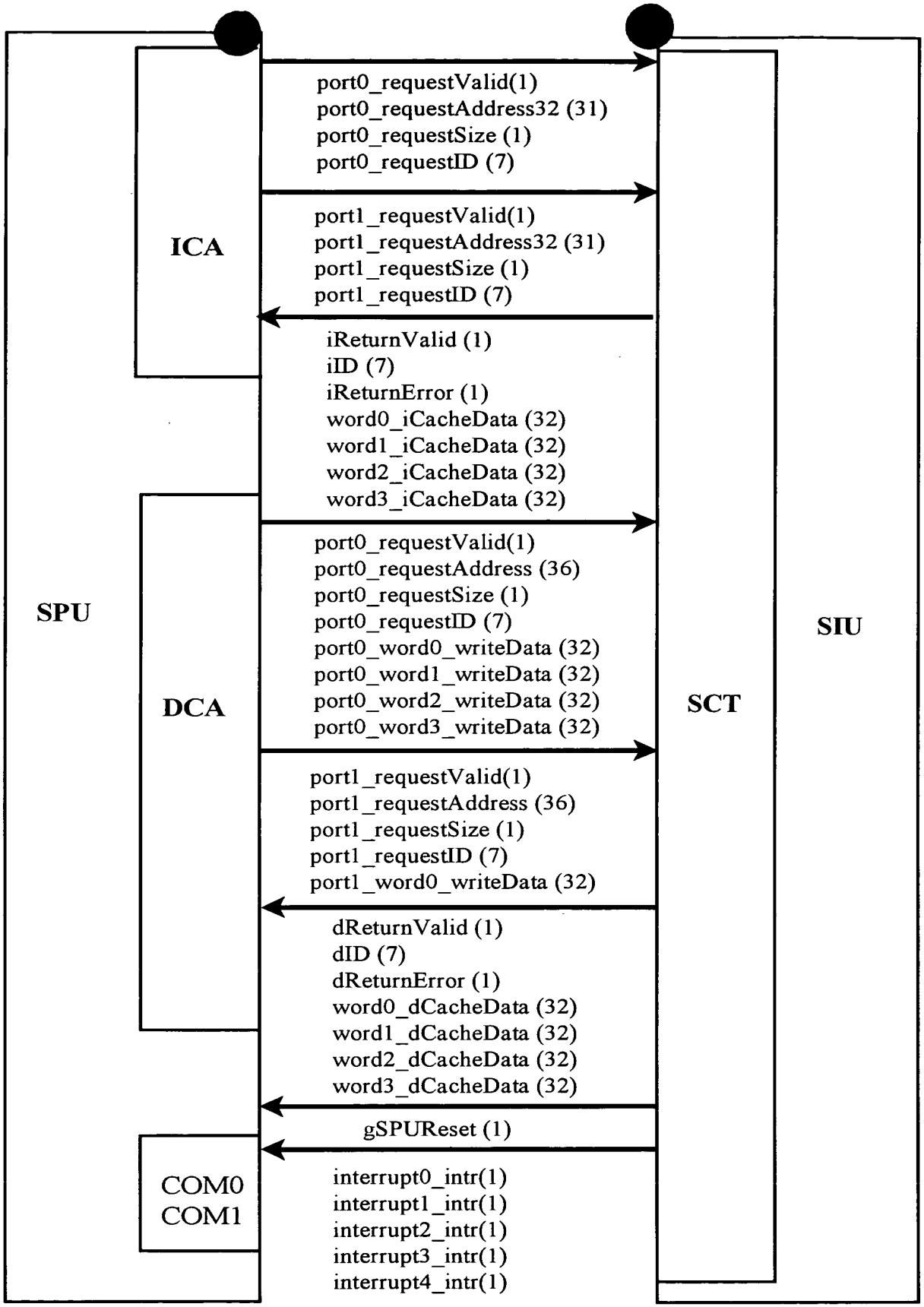
Global Extended Interrupt Pending Register

Fig. 18



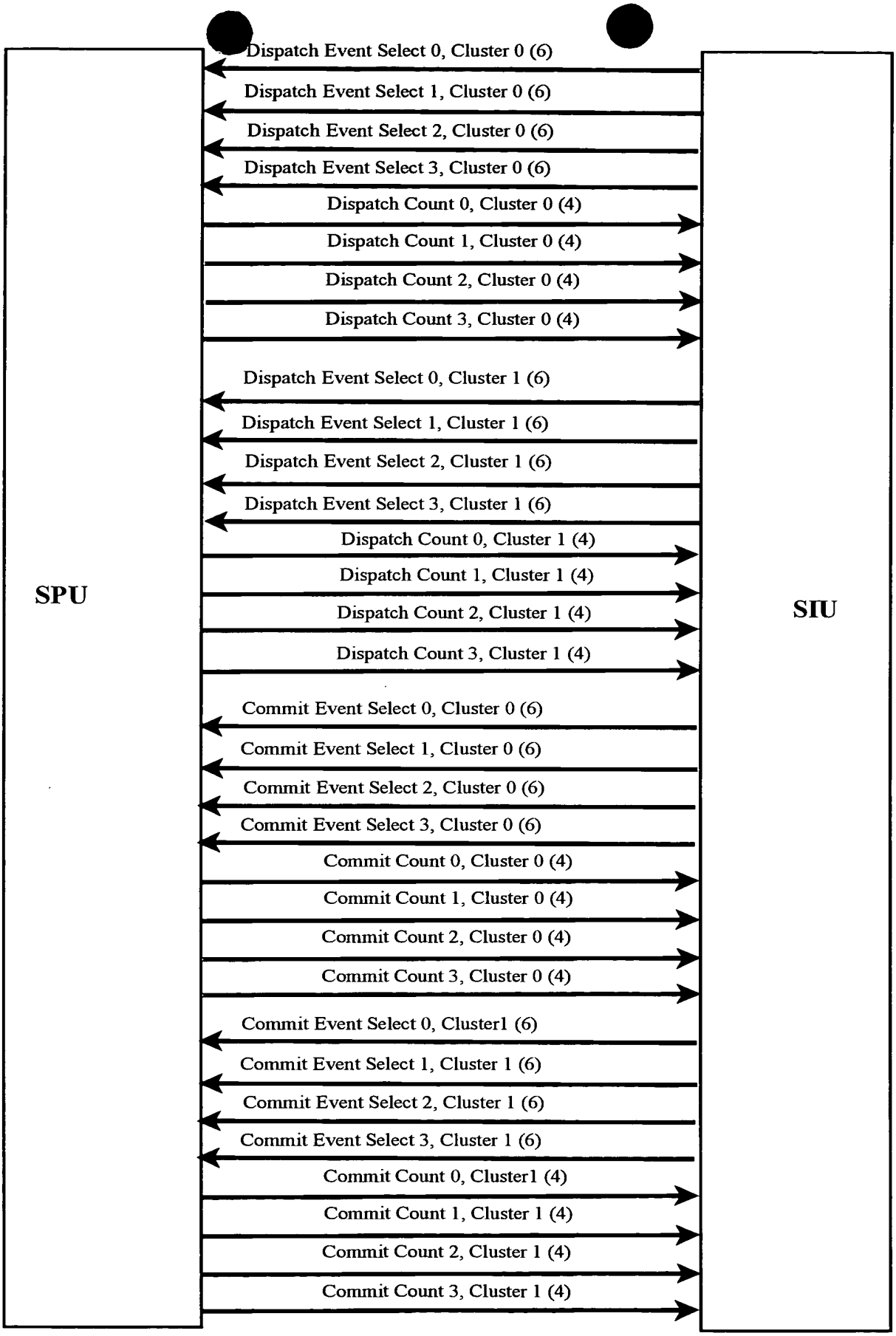
PMU/SPU Interface

Fig. 19



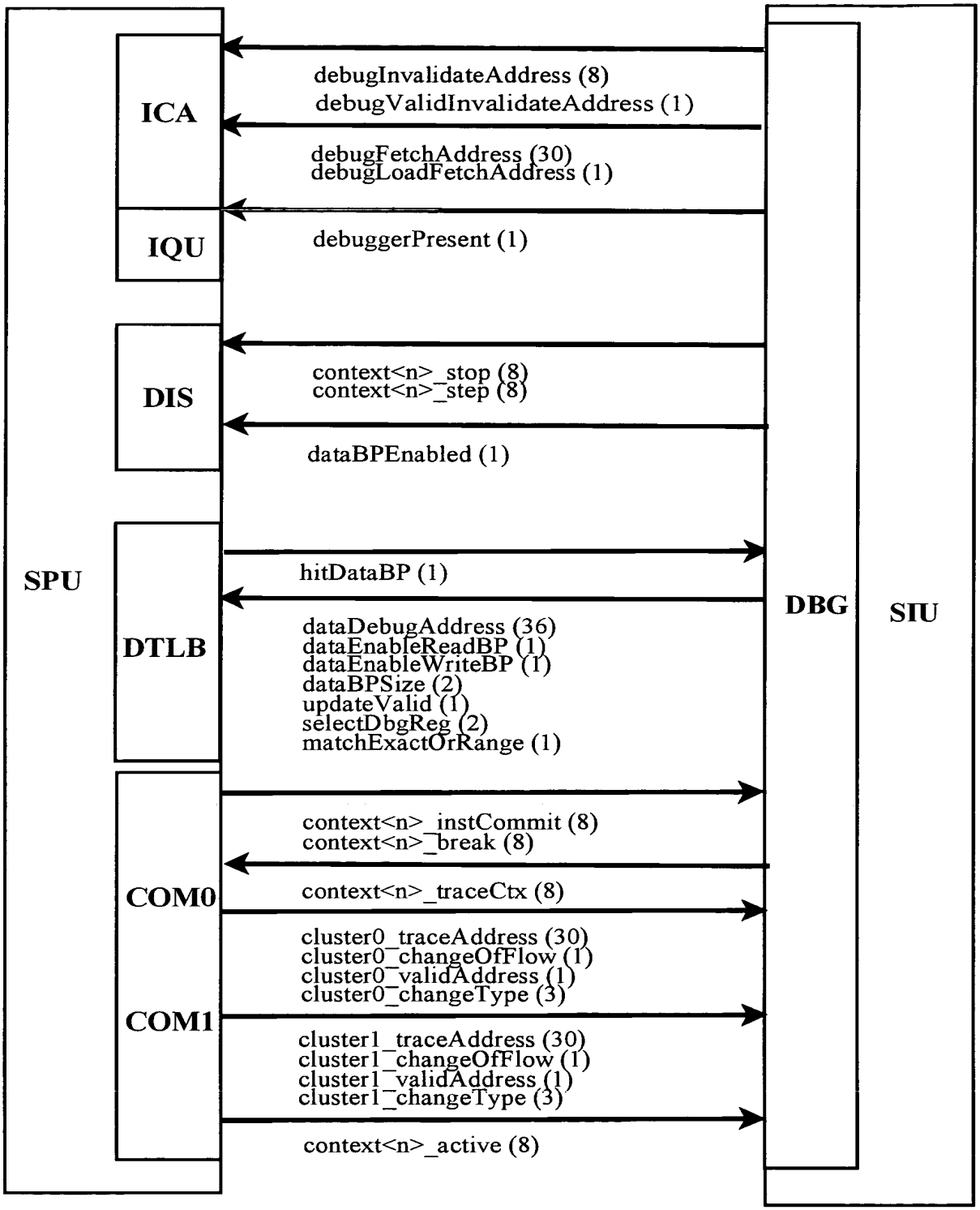
SIU/SPU Interface

Fig. 20



Performance Counter Interface

Fig. 21



SIU/SPU OCI Interface

Fig. 22

BEV	Cause	Virtual Address	Physical Address	Memory Type
1	Reset	BFC00000	01FC00000	uncached
1	TLB Refill	BFC00200	01FC00200	uncached
1	General	BFC00380	01FC00380	uncached
0	TLB Refill	80000000	0000000000	determined by KO
0	General	80000180	0000000180	determined by KO
0	XCInterrupt	80000480	0 000000480	determined by KO
0	Activation	(VA Configurable within the PMU)		

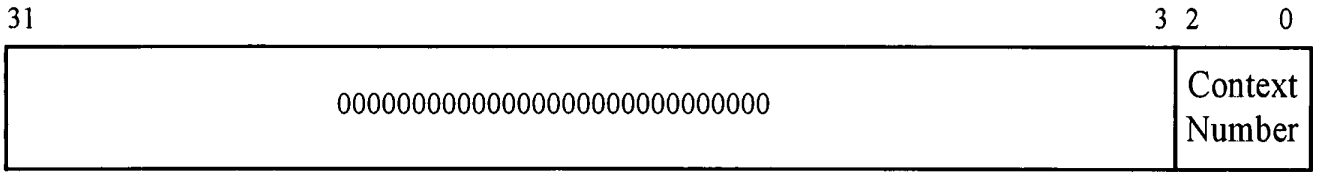
XCaliber Vectors

Fig. 23

Exceptions	Cause Code
Address Error - Instruction	4
Address Error - Data Load	4
Address Error - Data Store	5
TLB refill - Instruction	2
TLB invalid - Instruction	2
TLB refill - Data Load	2
TLB refill - Data Store	3
TLB invalid - Data Load	2
TLB invalid - Data Store	3
TLB modify - Data Store	1
Bus error - Instruction	6
Bus error - Data	7
Integer overflow	12
Trap	13
System Call	8
Breakpoint	9
Reserved instruction	10
Coprocessor unusable	11
Watch	23
Interrupt	0
XC Interrupt	0

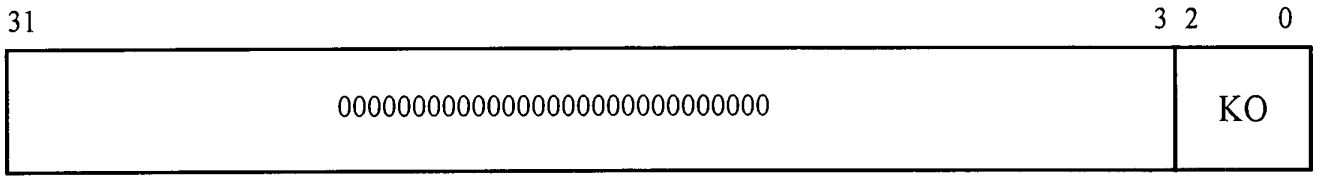
List of Vector Exceptions

Fig. 24



Context Number Register

Fig. 25



Config Register

Fig. 26

Current State	SIU Input	Dispatched one instruction this cycle	Next State
Run	Run	X	Run
	Idle	X	Idle
	Step	X	Stop
Run Idle	Run	X	Run
	Idle	X	Idle
	Step	X	Step
Step	Run	X	Run
	Idle	X	Idle
	Step	0	Step
	Step	1	Step_Idle
Step Idle	Run	X	Run
	Idle	X	Idle
	Step	X	Step_Idle

Operation of the OCI State Machine

Fig. 27

Bit Value	Type
000	Branch Not Taken
001	Branch Taken
010	JMP, ERET
011	Exception - TLB Refill
100	Exception - General Exception
101	Exception - Packet Load Exception
110	Exception - Extended Interrupt
111	Invalid

Fig. 28

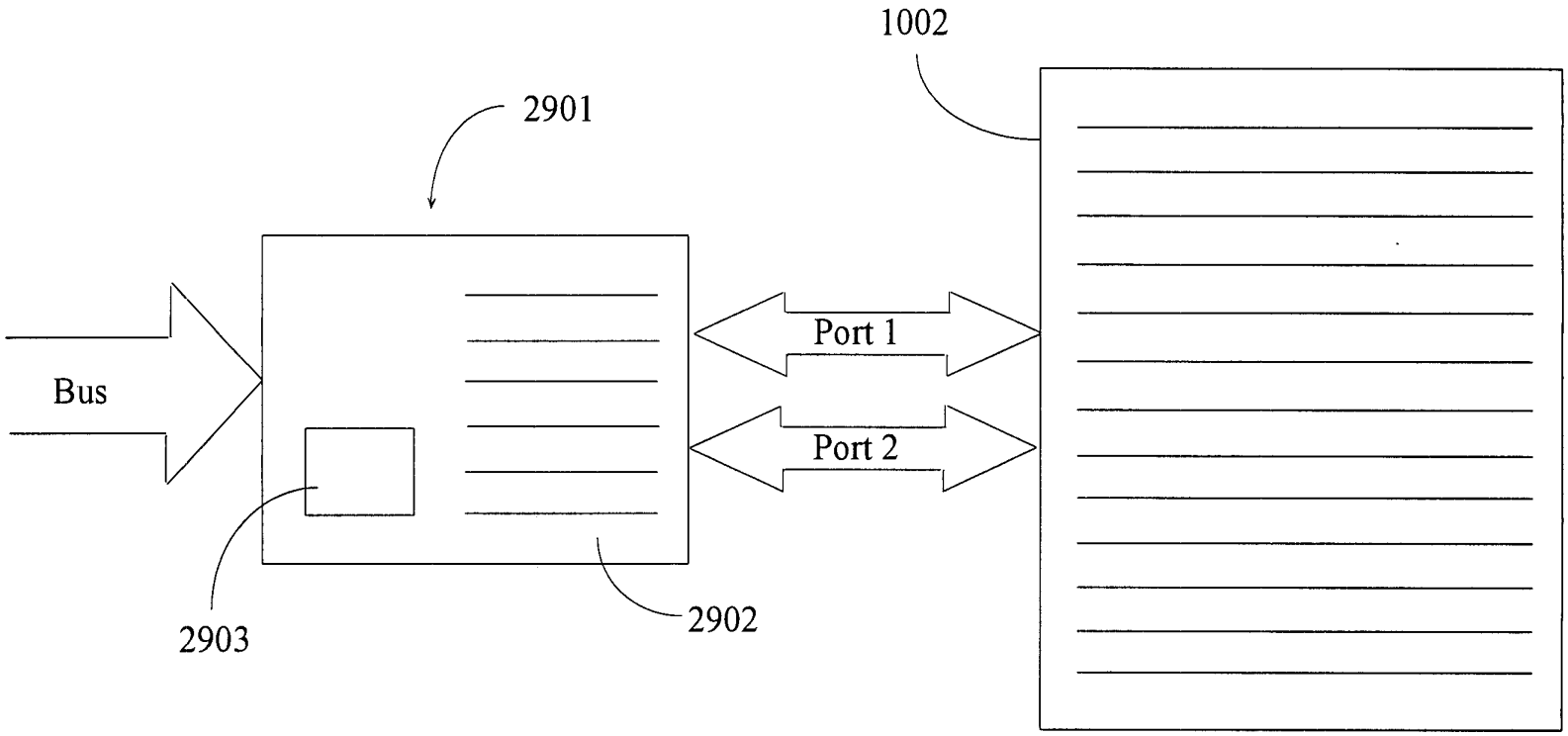


Fig. 29